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SERVICE MANUAL
MODEL B
CAPTURE TYPE
SOLID STATE

Console combination, Reversible and Sforzando actions.

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SOLID STATE COMBINATION ACTION
SERVICE MANUAL FOR MODEL B
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This paper is intended to explain, briefly, the manner in which the Model B combination memory system operates. It will further detail the service procedures which may be performed in the field. It is not intended that any field work be done on the printed circuit boards. Any printed circuit board repairs will be done at the factory where adequate facilities exist for such work.

Figure 1 is a block diagram of the Model B memory system. Central to the system is the memory chip (or chips), each of which is a group of 16 flip-flops within a small package. Each memory chip will retain memory for 16 different combinations. A combination is represented by the peculiar on-off status of stops which may be recalled by depressing a piston. A block diagram of a memory chip is shown in Figure 2.

Figure 2 will reveal that the 16 different pistons each utilize a distinct flip-flop within the package. The particular piston depressed will "address" its assigned flip-flop by the activation of the X-Y address lines. It may be seen that if X4 and Y1 are activated, flip-flop #1 will be addressed since it resides at the intersection of address lines X4 and Y1. By similar addressing, flip-flop #16 will be addressed when lines X1 and Y_1 are activated. In other words, each of the 16 pistons will refer to a different flip-flop within the memory chip and

will either "set" the status of a stop therein or will "read" or recover the status of the stop.

Referring again to Figure 1 it will be seen that each memory chip is not only "addressed" by a particular piston but is also told, via the "Write gates" or the "Read gates" whether we wish to "set" a combination or "Read" or recover a combination. Depressing the "set" piston activates the Write gates when a piston is depressed. If a piston is depressed and the "set" piston is not depressed then the "Read gates" are activated.

It will be noted that the pistons are shown connecting a "Piston common" lead to the "Address generation" block. When a piston on the Great manual is depressed, the piston simultaneously establishes an address within the memory chip and tells the Division Recognition block which group of Read gates is to be activated. In this case, only the Read gates for those chips which serve the Great manual will be activated. The result will be that all Read gates on the Great manual will be allowed to pass the remembered status of the Great combination to the Knob Actuator Drivers.

The knob actuator drivers are transistor chips which activate the kicker magnets or the solenoids which cause the knobs to move in or out. These transistors are operative only when the Read gates are activated. If a particular Read gate is not activated when a piston is depressed it will not allow that stop knob to be moved.

The Model B memory system is designed for eight different "piston commons". This allows up to eight different divisions to be serviced on an organ. One of these divisions is allocated to the "General" division. Whenever a piston is depressed which is connected to the General piston common lead, all stops in the organ will be affected since the general common allows all Read/Write gates to be activated at the same time. The other seven divisions are used, as required, for the different manuals and pedal divisions of the organ.

The following summarizes the operations which take place when "Reading" a combination.

1. The "Set: piston is not depressed. The control circuitry will allow only the "Read gates" to be activated when any piston is depressed.
2. A piston is depressed. (For example Great #2.) On the control board, piston diodes connected to piston #2 cause the address-line sink circuits for X4 and Y2 to be turned off. Turning off the sink circuits allows the X4 and Y2 lines to all memory chips in the system to rise from zero volts to nearly 5 volts. This means that every chip in the system has now presented, at its output terminals, what it has stored in its flip-flop at location 2.
3. When Great #2 piston was depressed, a current was also sent down the Great piston common line which tells the division recognition circuitry that it is being asked to open the "Read gates" for the Great division

chips, only. Opening the gates consists of changing the "Read" line to the gates from 5 volts to zero volts. When the gates are thus opened, the output from each of the Great memory chips is allowed to pass to the Transistor drivers for the Great knobs. The knobs will move to the position indicated by the stored combination.

4. When the division recognition circuitry caused the "Read gates" to be opened, the "Hold" circuitry also came into action. This circuitry is installed to keep the piston activated for a period of time sufficient to allow the knobs to complete their movements. Even had the piston been only "tapped", the hold circuit would keep the piston effectively depressed for a certain minimum period of time. This period of time is adjustable by a screwdriver adjustment on the control board.

5. The "Read" gates for the Great division will remain activated (held to zero volts) for as long as the piston is depressed or for as long as the hold circuit is adjusted to remain operative, whichever is longer. When the piston is released, or the hold times out, the read gates for the Great division will return to 5 volts, closing the gates for further change of the knob positions.

The following summarizes the operations which take place when writing (Setting) a combination.

1. The "Set" piston is depressed. This prepares the control circuitry to allow only "Write gates" to be activated. (No write gates are actually activated until a piston is depressed which will tell which write gates are to be opened).
2. A piston is depressed. (For example Swell #5). On the control board, piston diodes connected to piston terminal #5 cause the address-line sink circuits for X3 and Y4 to be activated. Turning off the sink circuits allows the X3 and Y4 address lines to all memory chips in the system to rise from zero volts to 5 volts. This means that every chip in the system has been addressed and has been prepared to accept a possible change of its #5 flip-flop status.
3. When Swell #5 piston was depressed, a current was also sent down the Swell division piston common line, telling the division recognition circuitry that it is being asked to open the "Write" gates for the Swell division, only. Opening the write gates consists of changing the Write line from 5 volts to zero volts.
4. Once the write gates have thus been opened, (for the Swell division only) the "position sense"

circuits will cause the #5 flip-flop in each of the Swell group memory chips to assume the state represented by the present position of the knob associated with each chip.

5. The piston, Swell #5, and the Set piston are now released. The memory chips have now stored the combination requested for the Swell division.

Operation of the General pistons may be different from that described, depending upon whether the particular system is one that allows a maximum of 16 pistons or one which allows a maximum of 32 pistons.

A system which is designed for 16 pistons will utilize one memory chip for each knob in the organ. The memory chip, containing 16 flip-flops, will thus handle the maximum of 16 pistons. In such a system the general pistons utilize (for an organ with 9 general pistons) the first 9 flip-flops within each memory chips. The remaining 7 flip-flops are then assigned to the division pistons. When such is the case the generals are designated pistons 1-9 and the divisional pistons are 10-16. In other words, in this model, the divisions are separated from the generals by address. The system, when wired, will return pistons 1-9 only to the general piston common and the remaining pistons will be returned to different division piston common lines. The division recognition circuitry will always associate pistons 1-9 as being a general and will cause Read/Write gates for all divisions to be affected when a general piston is depressed.

The same circuitry will recognize pistons 10-16 as being associated only with the division from which current is detected on a piston common line.

A system which is designed for 32 pistons will use two memory chips for each knob on the organ. One of the memory chips is assigned for the exclusive use of general pistons. A 32 piston model also uses an additional gate chip for each knob on the organ. A typical system will allow 16 general pistons and 16 division pistons. Since, as previously explained, depressing a piston establishes an address to all memory chips in the system, it becomes necessary to differentiate between general and division pistons by some means other than address. This determination is made by the division piston common lines (as before) along with the use of separate Read/Write gates for the generals and the divisionals. In other words, whenever a General piston is depressed, only the Read/Write gates for the added memory chips are activated. When a division piston is depressed, the Read/Write gates for only the proper division memory chips are activated. It will be noted, on the schematic diagram for the memory boards, Fig. 3, that a separate set of Read/Write lines is provided for the added memory chipand its associated gates.

The "Cancel" function is similar to a "Read" function with one exception: An address is not established to any of the memory chips. Instead, the output of all memory chips is caused to simulate an "off" command by the use of the cancel diodes. All chips in the system are given a simulated "off" output but only

those chips which are given the "Read" gate command are allowed to pass the "off" to the actuator transistors. A cancel is accomplished by simultaneously activating the cancel diodes and telling the division recognition circuitry which Read gates should be opened.

Schematic diagrams of the complete system are included in this manual for those who wish to follow the circuitry as described. The following relates the schematic diagrams to the various functions described heretofore.

Figure 3 is the schematic for one memory board. This schematic shows 1/6 of the circuitry of one board -- that for one of the 6 stops contained on one board. The kicker or solenoid circuit is shown in the upper left-hand corner of the drawing. This is the ultimate activator of the system. Figure 3 also shows the layout of parts for each 1/6 of the board with the various memory chips and gate chips identified. The schematic shows the 32 piston system. If the board is assembled for a 16 piston version, chips 2 and 4 are not included.

Figure 4 is the schematic of that part of the control board which accomplishes addressing of the memory chips. The terminals for the 16 pistons are shown at the left-hand edge of the page. This portion is further detailed in figure 4A, showing how the pistons are assigned for the 16 and 32 piston models. Figure 4 further details the "Hold" generator which is activated when any piston is depressed. When any piston is depressed, one of the X lines will be activated. The chip "W" (an "or" chip) starts the delay single-shot as soon as it sees one of the X lines

go to 5 volts. The delay single-shot outputs a pulse (variable length, depending upon adjustment) to the gate chips "U, T, and S. These chips (one circuit for each X and each Y line) have their outputs connected to the piston line for each X and Y line. If a particular chip circuit sees that its X or Y line has been activated and the hold signal is present, it holds the piston line for that piston to zero volts as long as the "Hold" signal persists. After the hold signal disappears, the piston line will return to normal if the piston is no longer being held down.

The address line "Sink Circuits" control the addressing of the memory chips. (See summary of Read/Write (set) operations on pages 3 through 6.

The purpose of the Sink Circuits is to change the X-Y lines, as required, from a Zero "at rest" voltage to approximately 4 volts when a piston is depressed. These circuits must be able to cause this change even though a large number of memory chips may be in use, ie, when a large amount of current must be controlled.

With all pistons "at rest" Q1 is in a saturated conducting condition since its base is being provided with drive current via the 330 ohm resistor connected to +5 volts. This base drive current is routed through two silicon diodes. Since Q1 is saturated (conducting) it causes Q2 to be turned on (saturated) also since Q2 is a PNP transistor. A PNP transistor will be in saturation when its base is tied to its collector. With Q2 saturated, any current which flows from the memory chips address line will be shunted directly to ground, causing that X or Y line to be essentially 0 volts.

When a piston is depressed (for example #15, which will call for X1 and Y3 to be addressed), the drive current being supplied to Q1 base on both X1 and Y3 sink circuits, will be diverted directly to ground, through one of the division recognition transistors. This diversion of Q1 base current will cause Q1 to become non-conducting. When Q1 stops conducting, Q2 will also become cut-off. When Q2, for both X1 and Y3, become cut-off, their respective address lines will rise to approximately 4 volts. This voltage is derived through the 680 ohm resistor which connects +5 volts to the address line.

It will be noted that the hold chip output, being connected to the piston line, will shunt the base current for Q1 in the same manner as a depressed piston thus holding the Sink Circuit open for at least as long as the hold time period.

The Cancel driver is also shown on Figure 4. This circuit causes the "Cancel Common" line to go to zero when the cancel piston is depressed. It also is subject to action of the hold circuit.

The cancel circuit operates in much the same manner as the Sink Circuits except that a NPN transistor is used for Q2. The NPN transistor will conduct (sink) the cancel buss to 0 volts only when the cancel piston is depressed. This is as opposed to the opposite action of the Sink Circuits. The NPN transistor at Q2 will <u>conduct</u> when Q1 is cut off.

Figure 5 is the schematic of the division recognition portion of the control board. This circuit sees current returning

from the pistons, on the piston common lines, and activates the Read/Write (set) lines -- depending upon whether the Set piston is depressed. It will be noted that the General piston common enters a circuit whose output activates the General Read/Write lines. If the system is wired for 16 pistons, the output of the General Read/Write lines is applied, via jumpers on the back panel, to auxiliary inputs on the other seven Read/Write gate drivers. In other words, if a General piston is depressed, on a 16 piston model, it simply causes all of the division Read/Write gate drivers to be actuated simultaneously.

It will be noted that the "Hold" signal is also applied to the Read/Write gate drivers. This is because it is necessary that the gates be held open as well as the address maintained, during the hold period. An address does nothing unless a gate is open at the same time.

POWER SUPPLY

Flip-Flop memory systems require that power be uninterrupted if memory is to be retained. Main power to the memory system is provided by a continuously energized 5 volt power supply. This power supply is backed up by a battery supply which will retain memory up to several hours if the commercial power is interrupted.

If commercial power is interrupted for more than 20 seconds, an alarm light on the console is lighted. This serves to alert the organist that a power interruption has occurred and that

combinations should be checked. If the battery was adequate for the period of interruption, no change in combinations will have occurred. The alarm light may be turned off by depressing the reset button, located adjacent to the alarm light.

In larger systems an auxiliary 5 volt supply is required. This auxiliary 5 volt supply will not be continuously operated but will come on only when the organ is turned on.

SERVICING INSTRUCTIONS

The solid-state combination system is made up of plug-in printed circuit boards. A spare memory board is furnished with each system. Servicing of the system will consist, primarily, of locating the defective memory board. Once located, the board is to be replaced with the spare and the defective board shipped to the factory for repair and return. The following instructions are intended to serve as a guide in locating defective memory boards and to help pinpointing other possible problems.

The proper board to be replaced, for those problems which might be caused by a defective memory chip or gate chip, may be identified by reference to the board index. This index is stored in the memory system housing and serves to relate the various stops, by name and division, to the board on which its circuitry is located. The boards are plugged into numbered slots in the memory housing and may be removed by using the board puller which is furnished with the system.

The following are symptoms which might exist due to a problem on one of the boards:

a. A knob flutters, in and out, when recalling a combination.

b. A stop may not be set "on", or "off".

c. A knob may not be cancelled.

d. A knob may always be driven "on" or "off", even with no piston depressed.

The above problems will probably be rectified if the appropriate board is replaced with the spare.

The following problems may indicate trouble on the control board. A spare is not normally provided for the control board. However, a replacement is available, on short notice, from the factory.

Problem A. An entire division, or general, will not operate properly, that is, stops will not "set" or "read" properly. This could be due to a Read gate line or Write gate line not changing from 5 volts to zero volts when a piston for a division is depressed.

Problem B. All pistons which use a given X or Y line do not operate. (For example, if pistons 1, 8, 9 and 16 exhibit the same problem, it is possible that the address sink circuit for address line Y1 is not operative.) Reference to the Block Diagram, Figure 2, will help in diagnosing such a problem. Correct operation of the X-Y line address sink circuits may be monitored via the test jacks on the front edge of the control board. These jacks are multi-colored and are labelled for each of the X-Y lines. Proper operation of the sink circuits is evidenced by the following voltage measurements, made with a voltmeter, between the jacks and ground (-).

With no pistons depressed, all X-Y lines should read approximately .25 volts, positive, with respect to ground. When a piston is depressed, one X and one Y line should change to approximately 4 volts positive, with respect to ground.

Failure of an X or Y line to rise to a voltage at least 2 volts above ground is indicative of trouble on that X or Y line.

This problem is not necessarily due to a defective control board -- it could be caused by a peculiar defect in one of the memory chips on one of the memory boards. Before concluding that trouble exists on the control board, the following procedure should be followed.

1. Lock one of the defective pistons in the depressed position.
2. Attach the voltmeter to the X or Y line which is failing to rise above 2 volts (minimum).
3. Pull out the memory boards, one at a time, while watching the voltmeter. If no change is noted, plug the board back in and proceed to the next board. If the trouble exists on one of the boards, it will reveal itself as a sudden rise in the X or Y voltage when the board is removed. Such a defective board should be replaced with the spare.

Problem C. Knobs do not complete movement when piston is depressed briefly. This problem could be with the "hold" circuit. A test jack is provided for testing the hold action. A voltmeter should show approximately 4 volts, at the hold test-point, when a piston is depressed. The voltage should remain at 4 volts for approximately $\frac{1}{4}$ second (depending upon adjustment of the hold potentiometer).

Problem D. No cancel function. The cancel sink circuit may be monitored at test point provided on control board. The voltage at cancel test point should be approximately 5 volts with cancel piston at rest and approximately .25 volts with cancel piston depressed.

Problem E. Complete failure of the combination system will result if the 5 volt power supply fails. The 5 volts may be checked at the blocks mounted on rear wall of the console. These blocks are labelled +5 and -5 and a voltmeter should show at least 5 volts at this point. (The voltage is adjusted, at installation, to be exactly 5 volts, at the memory enclosure). Some systems use an auxiliary 5 volt power supply which is terminated on blocks marked +5 volts, control. This voltage must also be present for operation of the combination system.

All servicing of the combination system must be done with an approved voltmeter, only. Such a voltmeter would be a Simpson model 260, Eico model 567, or equivalent. Under no circumstances should a buzzer or other test instruments be used.

Any defective memory board which is replaced by the spare should be returned to the factory for repair. A note should accompany the board describing the nature of the problem which existed with the defective board in place.

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